

## MAR 2 3 2006 W

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

HATAKENAKA et al.

Application No. 09/871,978

Filed: June 4, 2001

For: SEMICONDUCTOR INTEGRATED

CIRCUIT DEVICE COMPRISING RAM WITH COMMAND DECODE SYSTEM AND LOGIC CIRCUIT INTEGRATED INTO A SINGLE CHIP AND TESTING

METHOD OF THE RAM WITH COMMAND DECODE SYSTEM

Allowed: January 4, 2006

Confirmation No.: 5265

Art Unit: 2133

Examiner: David TON

## SUBMISSION OF FORMAL DRAWINGS

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Issue Fee
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Attn: Official Draftsman

Dear Sir:

Applicants enclose herewith fifteen (15) sheets of formal drawings and request that the same be made of record in this application as a substitute for the informal drawings filed with the application on June 4, 2001.

Respectfully submitted,

deffrey A. Wyand, Reg. No. 29,458

LEXING, VOIT & MAYER

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Date:

Drawings - Formal (Revised 1/14/05)